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(54) Public telephone set

(57) There are provided a keyboard including a plurality of keys, a first memory device for storing a signal related to a dial number produced as a result of operation of said keyboard, a second memory device for storing a predetermined specific dial number, a control unit for comparing the contents of the first and second memory devices according to a predetermined sequence, and means controlled by the control unit for controlling transmission of a dial signal of the specific dial number when the contents of both memory devices coincide with each other. According to this invention it is possible to readily change such specific dial numbers as a rate free number or a number inhibited from transmitting its dial pulses.

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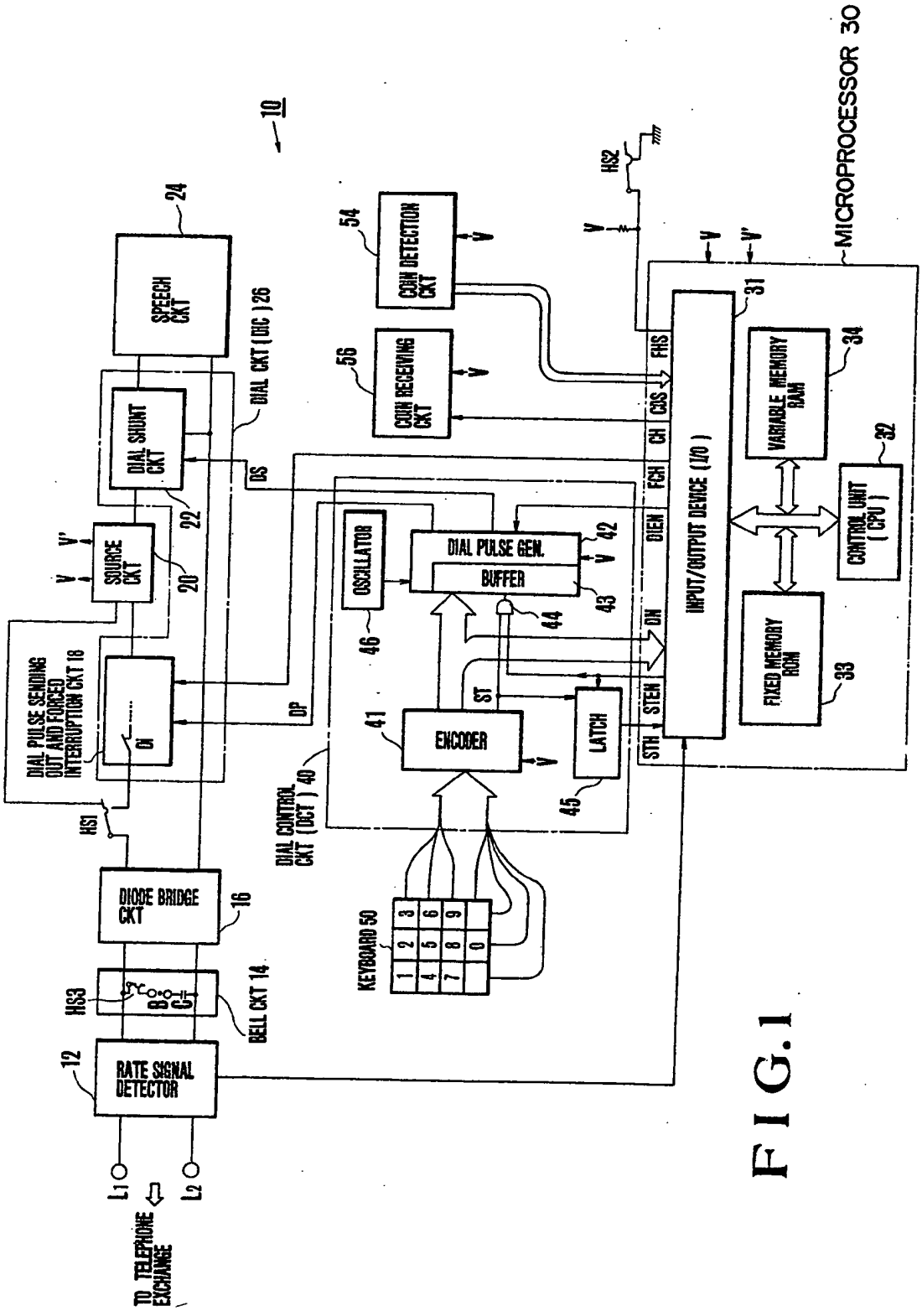

FIG.1

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FIG.2

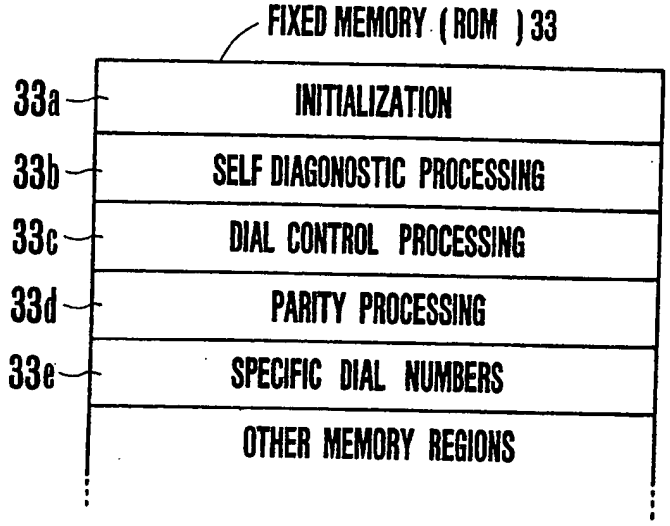


FIG.3

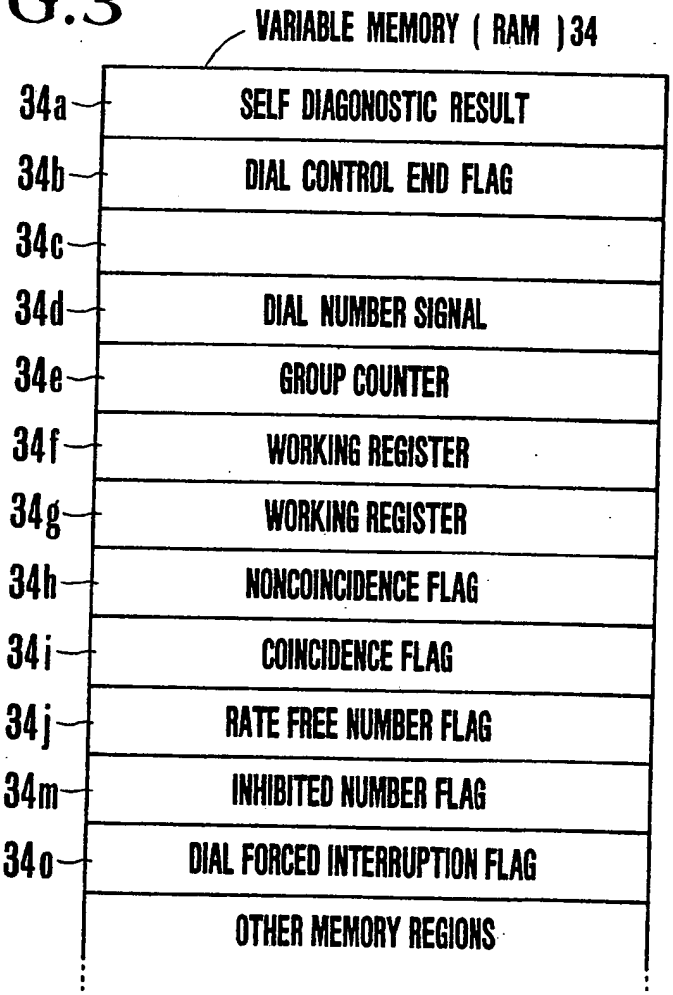
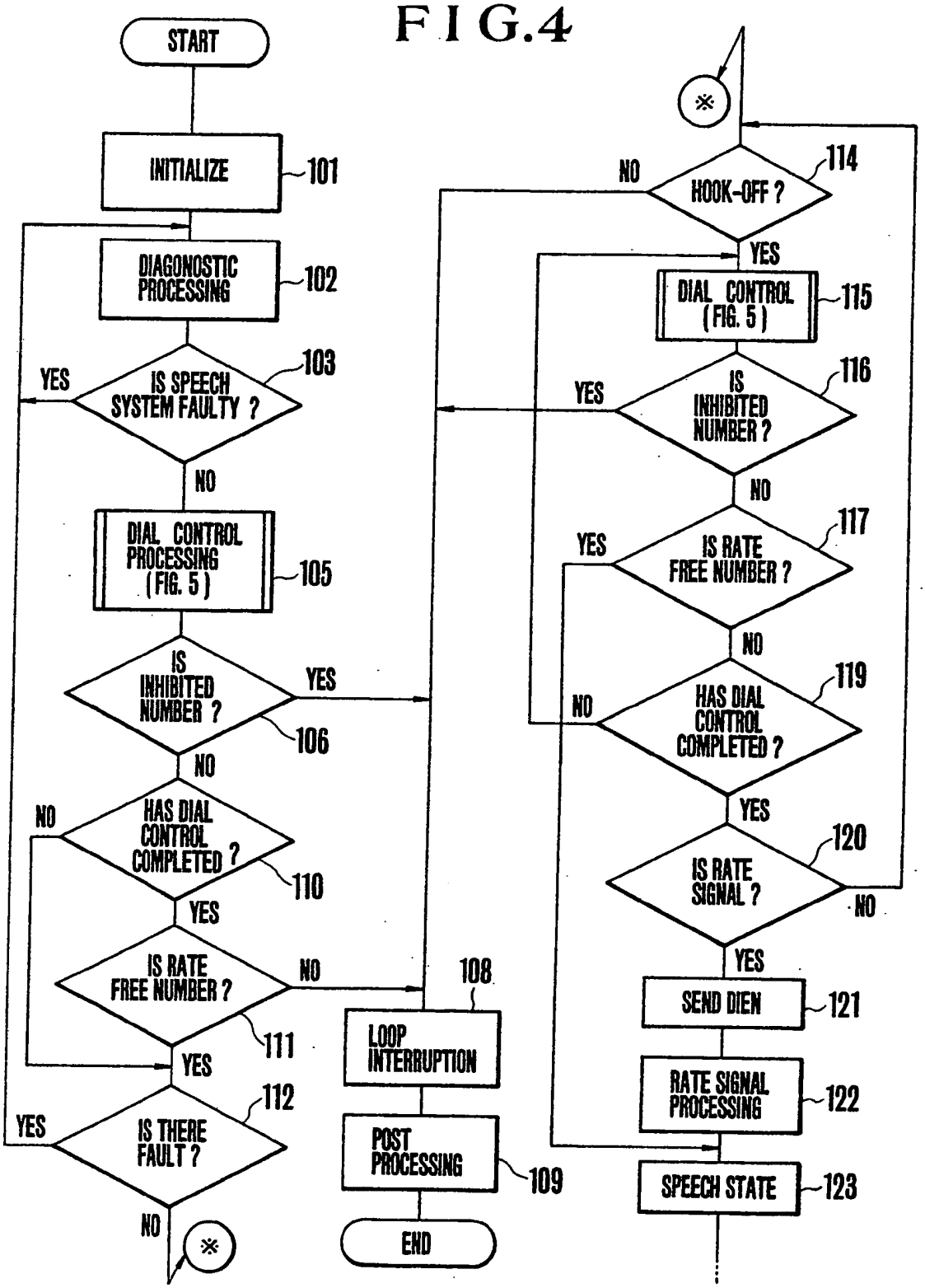


FIG.4


START
INITIALIZE
101
DIAGONOSTIC PROCESSING
102
IS SPEECH SYSTEM FAULTY ?
103
YES
NO
DIAL CONTROL PROCESSING (FIG. 5)
105
IS INHIBITED NUMBER ?
106
YES
NO
HAS DIAL CONTROL COMPLETED ?
110
NO
YES
IS RATE FREE NUMBER ?
111
NO
YES
IS THERE FAULT ?
112
YES
NO
※
LOOP INTERRUPTION
108
POST PROCESSING
109
END
※
HOOK-OFF ?
114
NO
YES
DIAL CONTROL (FIG. 5)
115
IS INHIBITED NUMBER ?
116
YES
NO
IS RATE FREE NUMBER ?
117
YES
NO
HAS DIAL CONTROL COMPLETED ?
119
NO
YES
IS RATE SIGNAL ?
120
NO
YES
SEND DIEN
121
RATE SIGNAL PROCESSING
122
SPEECH STATE
123

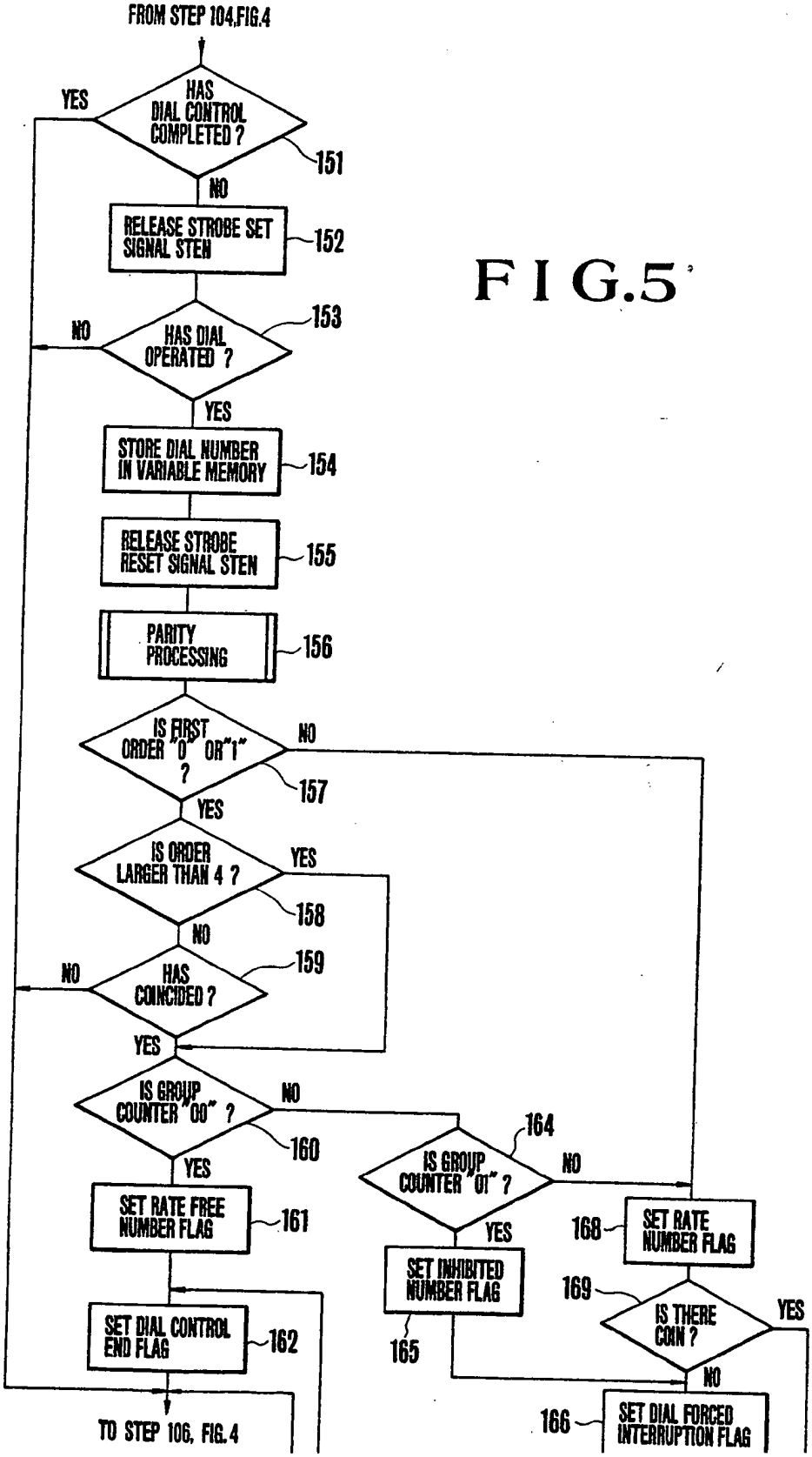

FROM STEP 104,FIG.4
HAS DIAL CONTROL COMPLETED ?
151
YES
NO
RELEASE STROBE SET SIGNAL STEN
152
HAS DIAL OPERATED ?
153
NO
YES
STORE DIAL NUMBER IN VARIABLE MEMORY
154
RELEASE STROBE RESET SIGNAL STEN
155
PARITY PROCESSING
156
IS FIRST ORDER "0" OR "1" ?
157
NO
YES
IS ORDER LARGER THAN 4 ?
158
YES
NO
HAS COINCIDED ?
159
NO
YES
IS GROUP COUNTER "00" ?
160
NO
YES
SET RATE FREE NUMBER FLAG
161
SET DIAL CONTROL END FLAG
162
TO STEP 106, FIG. 4
IS GROUP COUNTER "01" ?
164
NO
YES
SET INHIBITED NUMBER FLAG
165
168
SET RATE NUMBER FLAG
169
IS THERE COIN ?
YES
NO
166
SET DIAL FORCED INTERRUPTION FLAG

FIG.5

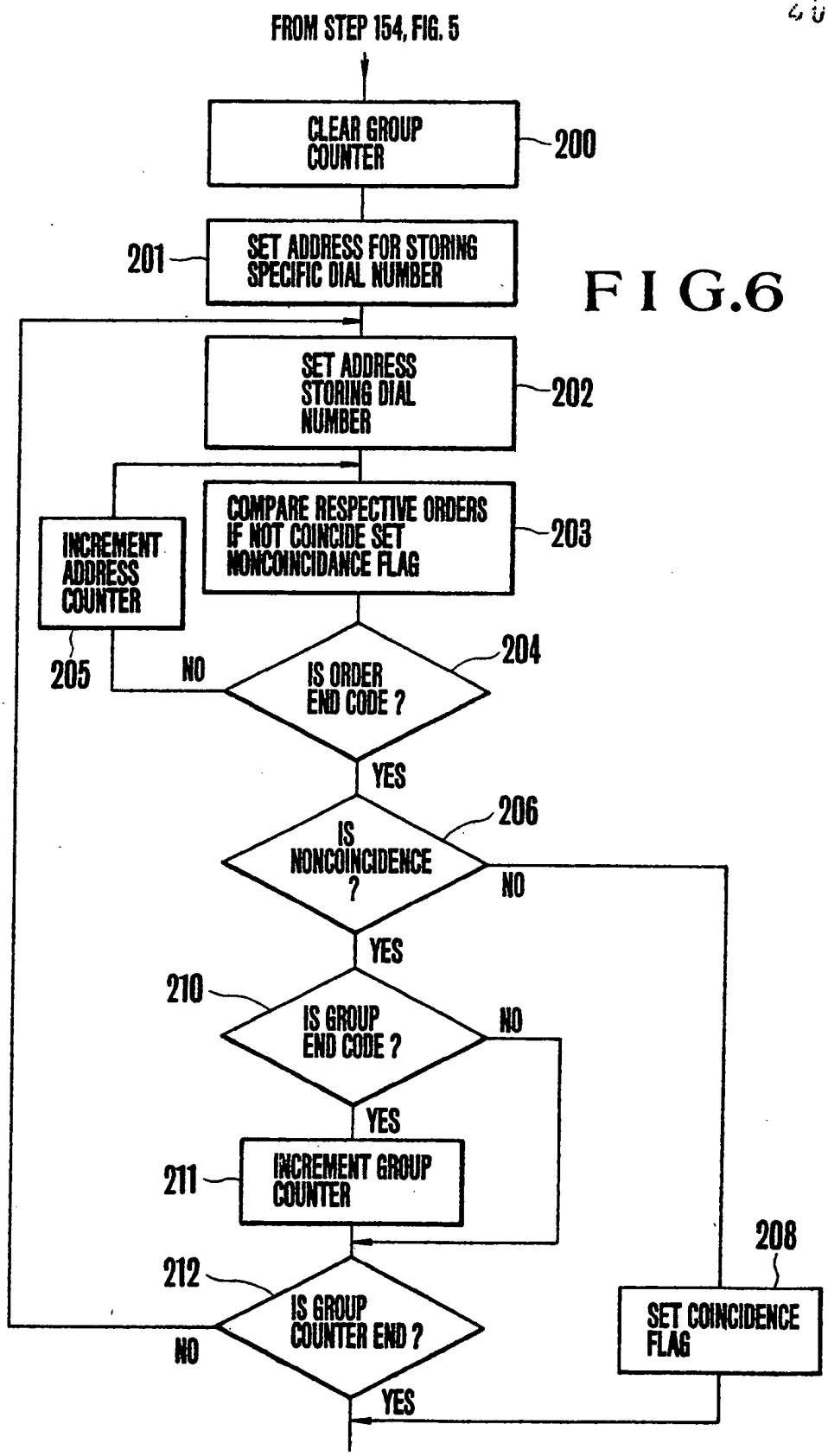

FROM STEP 154, FIG. 5
CLEAR GROUP COUNTER
200
SET ADDRESS FOR STORING SPECIFIC DIAL NUMBER
201
SET ADDRESS STORING DIAL NUMBER
202
COMPARE RESPECTIVE ORDERS IF NOT COINCIDE SET NONCOINCIDANCE FLAG
203
INCREMENT ADDRESS COUNTER
205
IS ORDER END CODE ?
204
NO
YES
IS NONCOINCIDENCE ?
206
NO
YES
IS GROUP END CODE ?
210
NO
YES
INCREMENT GROUP COUNTER
211
IS GROUP COUNTER END ?
212
NO
YES
SET COINCIDENCE FLAG
208

FIG.6

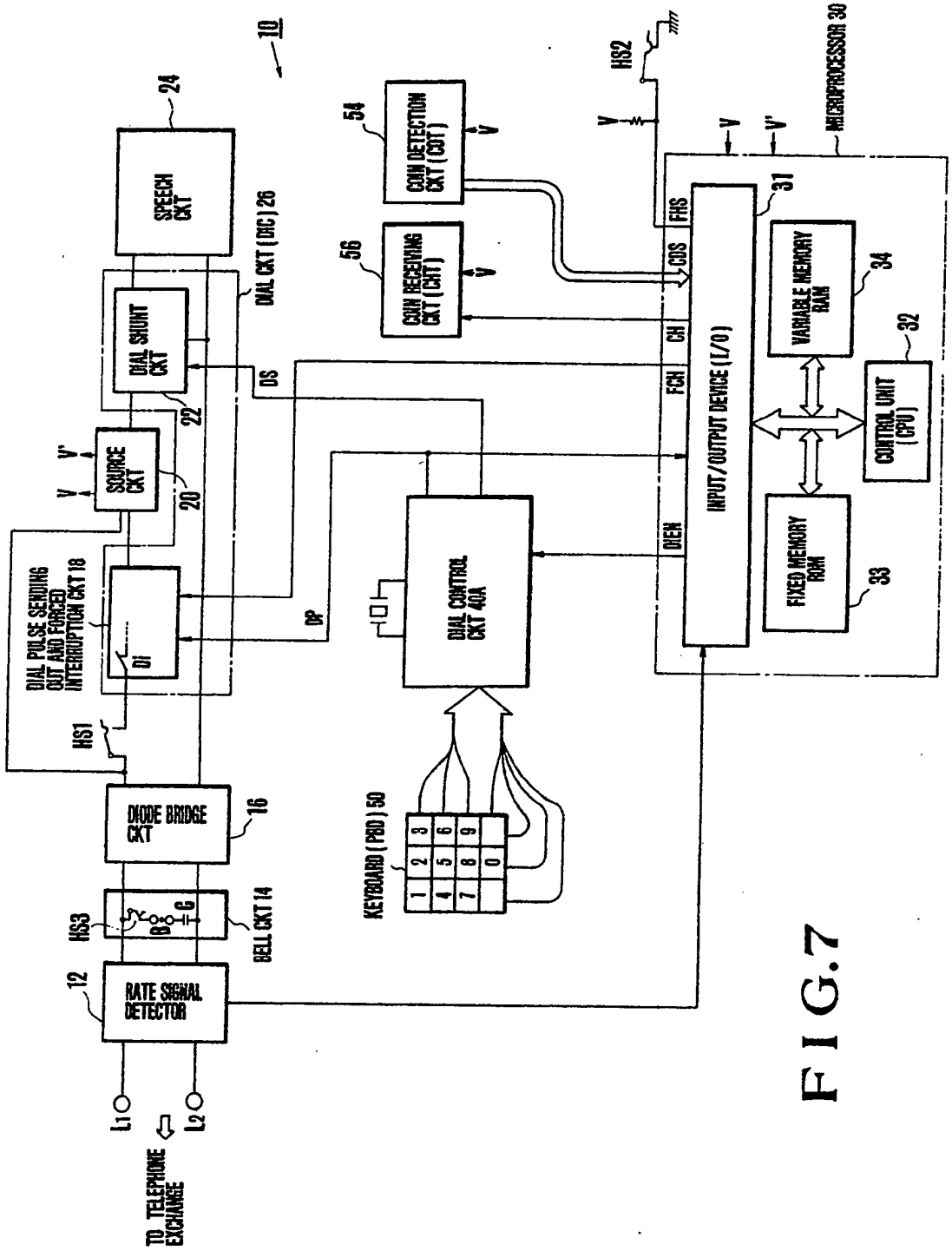

10
24
SPEECH CKT
DIAL CKT (DIC) 26
DIAL SHUNT CKT
22
DS
SOURCE CKT
20
V
V'
DIAL PULSE SENDING CUT AND FORCED INTERRUPTION CKT 18
DI
DP
HS1
DIODE BRIDGE CKT
16
HS3
BELL CKT 14
12
RATE SIGNAL DETECTOR
L1
L2
TO TELEPHONE EXCHANGE
54
COIN DETECTION CKT (CDT)
56
COIN RECEIVING CKT (CRT)
HS2
MICROPROCESSOR 30
31
FHS
CDS
CH
FCN
DIEN
INPUT/OUTPUT DEVICE (I/O)
VARIABLE MEMORY RAM
34
32
CONTROL UNIT (CPU)
FIXED MEMORY ROM
33
DIAL CONTROL CKT 40A
KEYBOARD (PBD) 50
1 2 3
4 5 6
7 8 9
0

FIG.7

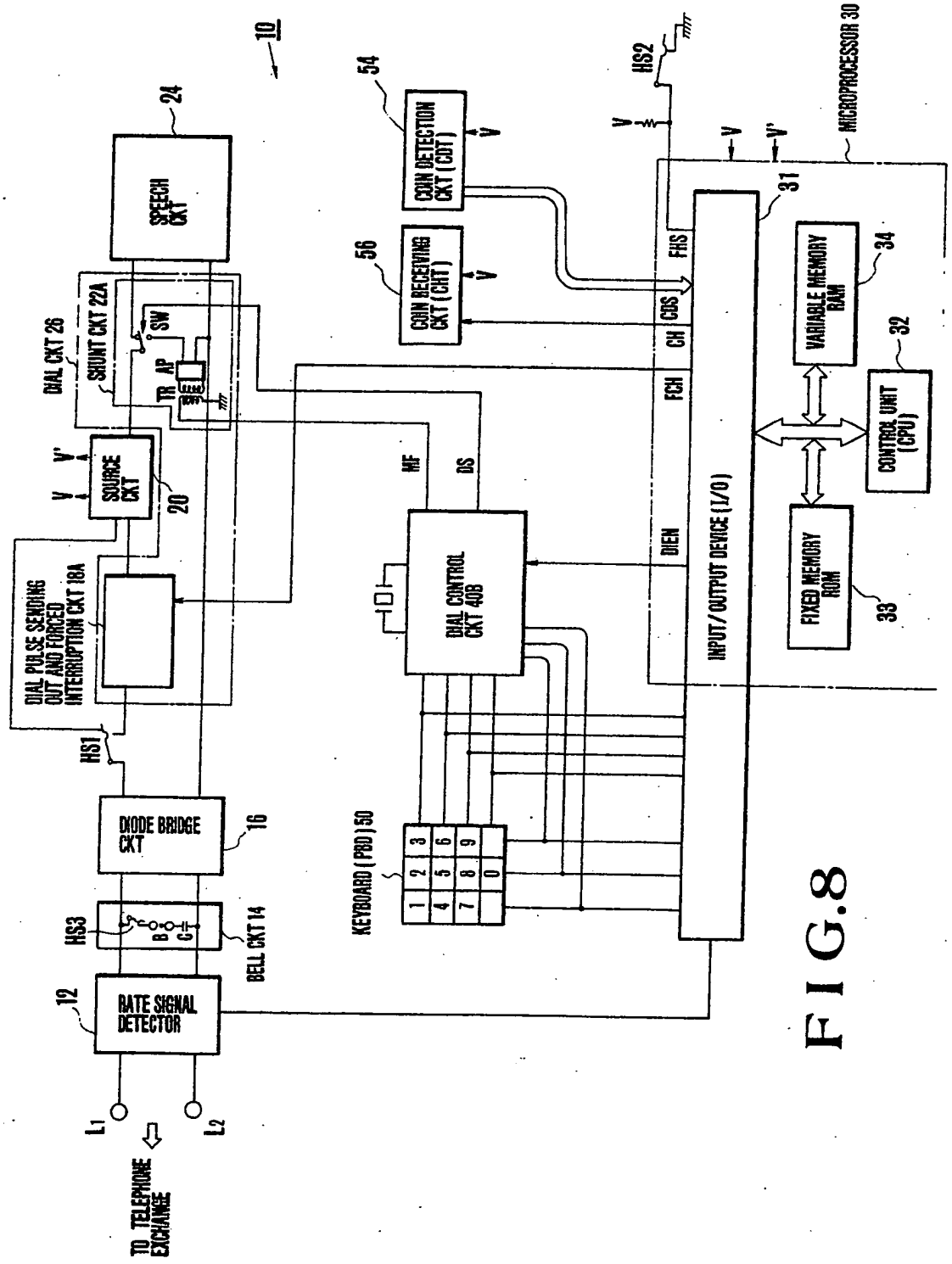

10
SPEECH CKT
24
SHUNT CKT 22A
DIAL CKT 26
SW
TR
AP
SOURCE CKT
20
V
V'
DIAL PULSE SENDING OUT AND FORCED INTERRUPTION CKT 18A
HS1
DIODE BRIDGE CKT
16
HS3
BELL CKT 14
RATE SIGNAL DETECTOR
12
L1
L2
TO TELEPHONE EXCHANGE
KEYBOARD (PBD) 50
DIAL CONTROL CKT 40B
MF
DS
CONN DETECTION CKT (CDT)
54
CONN RECEIVING CKT (CHT)
56
HS2
MICROPROCESSOR 30
INPUT/OUTPUT DEVICE (I/O)
31
FHS
CDS
CH
FCH
DIEN
VARIABLE MEMORY RAM
34
CONTROL UNIT (CPU)
32
FIXED MEMORY ROM
33

FIG.8

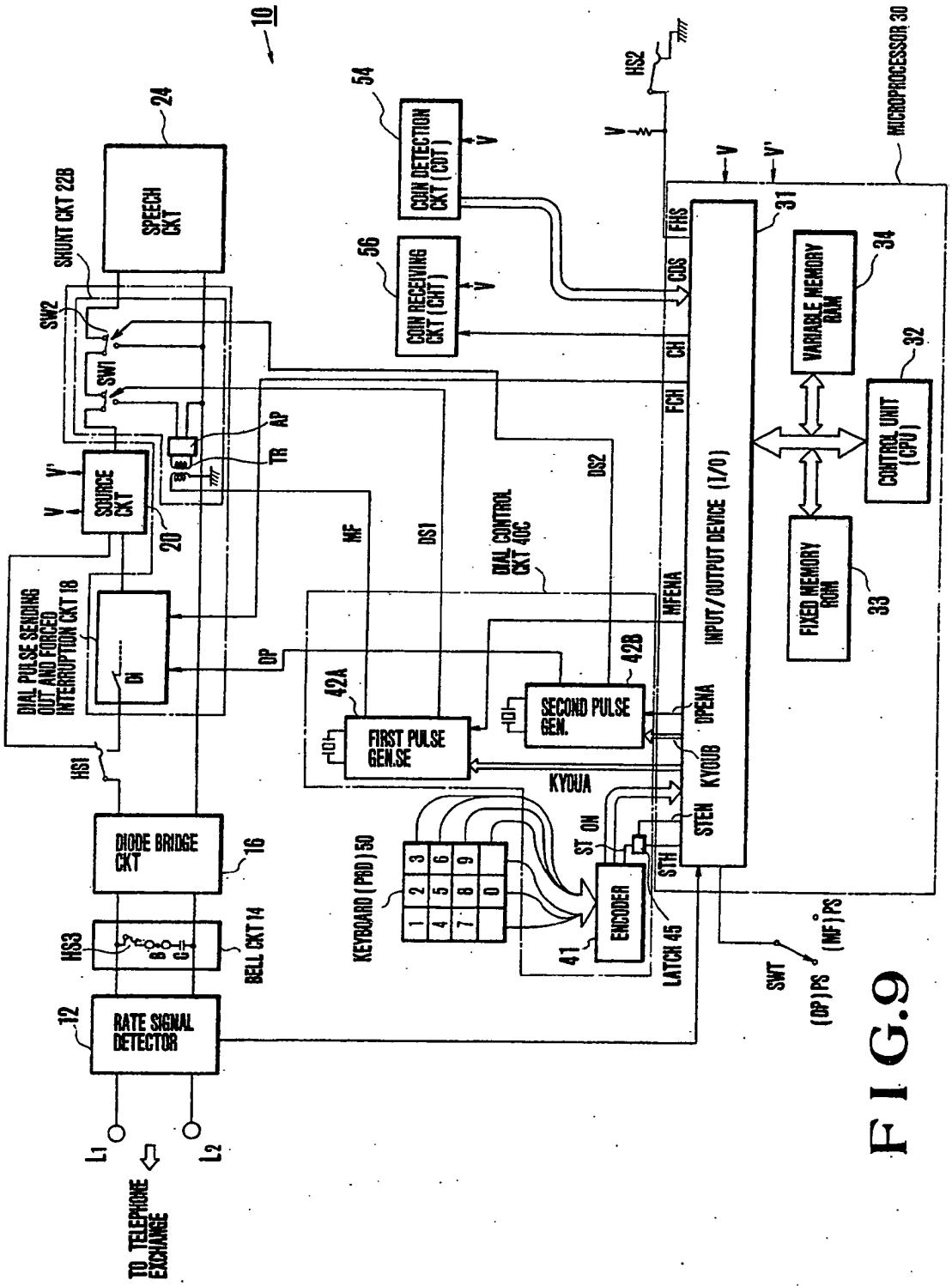

10
MICROPROCESSOR 30
INPUT/OUTPUT DEVICE (I/O)
CONTROL UNIT (CPU)
VARIABLE MEMORY RAM
FIXED MEMORY ROM
SPEECH CKT
SHUNT CKT 22B
SOURCE CKT
DIAL PULSE SENDING OUT AND FORCED INTERRUPTION CKT 18
DIODE BRIDGE CKT
BELL CKT 14
RATE SIGNAL DETECTOR
COIN DETECTION CKT (CDT)
COIN RECEIVING CKT (CRT)
DIAL CONTROL CKT 40C
FIRST PULSE GEN.SE
SECOND PULSE GEN.
KEYBOARD (PBD) 50
ENCODER
LATCH 45
TO TELEPHONE EXCHANGE
L1
L2
SW1
SW2
HS1
HS2
HS3
TR AP
DP
MF
DS1
DS2
KYOUA
KYOUB
STEN
STH
ST ON
DPENA
MFENA
FHS
CDS
CRS
FCH
SWT
(DP) PS
(MF) PS

FIG.9

SPECIFICATION

Public telephone set

This invention relates to a public telephone set, and more particularly a public telephone set which permits rate free signal transmission at the time of originating a specific dial number, but which disables the transmission of the signal at the time of originating another specific dial number or converts it to another dial number.

Usually, in a public telephone set, a dial tone transmission is made possible by lifting the receiver, i.e. a hook-off operation followed by insertion of a coin. However, it is necessary to permit dial tone transmission as well as rate free speech in the case of an emergency call for example to police, fire or ambulance services.

Moreover, in a public telephone set exclusively used in a city or a local area it is necessary to make it impossible to call a toll number or to send a signal to a toll repeater for the purpose of preventing toll speech. A public telephone set capable of providing such performance by an electronic circuit is disclosed in Japanese Patent Application Specification No. 152575/1978 (Japanese Laid Open Patent Specification No. 11648/1980) entitled Dial Number Control Circuit, filed by the same applicant.

That control circuit, however, comprises various hardware logic circuits such as a counter, a decoder, etc., so that such control circuit has to be strapped across strap terminals according to a specific dial number for which a rate free signal transmission is to be permitted or inhibited. Moreover the number of digits of a specific dial number is limited by the construction so that such control circuit is only applicable to a specific dial number of a specific number of digits and it is necessary to change a strap between strap terminals according to an area in which the telephone set is installed. In other words, the field of application of such control circuit is limited and its handling is troublesome.

Furthermore, the number of component parts of such a control circuit increases according to the number of digits of the specific dial number which not only complicates the circuit construction, but also increases the cost of manufacturing.

An object of this invention is to provide an improved public telephone set capable of readily and simply determining and changing, when desired, such specific dial numbers as a rate free number, and a dial number whose dial tone transmission should be inhibited.

Briefly stated, according to this invention a microprocessor is provided, a predetermined specific dial number is prestored in a memory device, and a dial number produced as a result of dial operation is stored in another memory device. The specific dial number is compared with a sent out dial number in accordance with the contents of respective memory devices and when these two dial numbers coincide with each other a control is made corresponding to the specific dial number.

According to this invention there is provided a public telephone set comprising a keyboard including a plurality of keys, a first memory device for storing a signal related to a dial number produced as a result of operation of one of the keys, a second memory device for storing a predetermined specific dial number, a control unit for comparing contents of the first and second memory devices according to a predetermined sequence, and office line originating means controlled transmission of a dial signal corresponding to the specific dial number when the contents of the first and second memory devices coincide with each other.

In the accompanying drawings:

Fig. 1 is a block diagram showing an embodiment of a public telephone set according to this invention;

Fig. 2 is a chart showing one example of the content of a fixed memory device shown in Fig. 1;

Fig. 3 is a chart showing one example of the content of a variable memory device shown in Fig. 1;

Fig. 4 is a flow chart showing the processing sequence of the public telephone set shown in Fig. 1;

Fig. 5 is a flow chart showing a detail of the dial control processing steps shown in Fig. 4;

Fig. 6 is a flow chart showing a detail of a parity processing step shown in Fig. 5; and

Figs. 7 through 9 are block diagrams showing modified embodiments of the public telephone set according to this invention.

Fig. 1 is a block diagram showing the basic construction of the public telephone set embodying the invention. A public telephone set 10 shown therein includes office line terminals L1 and L2 leading to a telephone exchange, not shown, via office lines. Accross the line terminals L1 and L2 are connected a rate signal detector 12 which detects a rate signal sent from the telephone exchange; a bell circuit 14 constituted by serially connected hook switch HS3, a bell B and a capacitor C and operates to inform a termination; a diode bridge circuit 16; a hook switch HS1; a dial pulse sending out and forced interruption circuit 18, a source circuit 20; a dial shunt circuit 22 and a speech circuit 24, in the order mentioned. The circuits 18 and 22 constitute a dial circuit (DIC) 26 which operates to send out the dial pulse from the telephone set, prevents propagation of pulse noise caused by the dial pulse to the speech circuit 24 and to forcibly interrupts originating of a dial number which should not be sent from the telephone set, and the operation of the dial circuit 26 is controlled by a dial pulse DP, a dial shunt signal DS and a forced interruption signal FCH which are sent from a circuit to be described later. The hook switch HS1 is normally open, but closed upon hook-off to form a DC loop circuit for the office line terminals L1 and L2 including the dial circuit 26 and the speech circuit 24. The purpose of the source

circuit 20 is to supply necessary power to various circuit elements comprising the telephone set. When the hook switch HS1 is open, that is at the time of hook-on, the output that is at the time of hook-on, the output of the diode bridge circuit 16 is applied to the source circuit 20 via the hook switch HS1 so as to cause the source circuit 20 to produce a source voltage V utilized as the back-up voltage of a variable memory device of a microprocessor 30 to be described later. In this case the source circuit 20 is supplied with a current of the order of several milliamperes from the diode bridge circuit 16. A capacitor, not shown is normally charged with this current to produce this source voltage V'. When the hook switch HS1 is closed, the source circuit 20 produces another voltage V for energizing other circuit elements in addition to the voltage V'.

This circuits 18, 22 of the dial circuit 26 will now be described. The dial pulse sending out and forced interruption circuit 781 hereinafter abbreviated as a dial tone sending out circuit opens and closes a dial switch D1 connected in series with the DC loop circuit in accordance with a series of dial pulses DP supplied from a dial control circuit 40 for sending out dial pulses DP to the telephone exchange, not shown, through the orifice line terminals L1 and L2. Furthermore, the circuit 18 is connected to receive a forced interruption signal to be described later from a microprocessor 30 to open the DC loop for resetting the telephone exchange.

The dial shunt circuit 22 is connected to receive a shunt signal from the dial control circuit 40 to short circuit the input terminals of the speech circuit 24 so as to prevent a pulse noise produced at the time of sending out the dial pulses from affecting the speech circuit 24.

As well known in the art, the microprocessor 30 is constituted by an input/output device (I/O) 31, a central processing unit (CPU) 32 in the form of a read only memory (ROM) device, for example, a fixed memory device 33, in the form of a random access memory device (RAM), for example, for storing predetermined data, instructions and other informations, and a variable memory device 34 made up of a plurality of registers which stores the results of processings executed under the control of the central processing unit 32 based on the informations from a counter and the fixed memory device 33. The details of the fixed memory device 33 and the variable memory device 34 are shown in Figs. 2 and 3 respectively.

In the public telephone set described herein a keyboard (KBD) 50 is used having a matrix of 3 x 4. All outputs of the keyboard 50 are applied to the encoder 41 of the dial control circuit 40. The encoder 41 applies a digital number signal DN of a 4 bit construction, for example, corresponding to depressed keys to a buffer circuit 43 of a dial pulse generator 42, and to the I/O device 31 of the microprocessor 30. When a key of the keyboard 50 is operated, the encoder produces a key-on signal ST in addition to the digital number signal DN described above, these signals being sent to an AND gate circuit 44 and a latch circuit 45. As the encoder 41 may be used type MC14419IC manufactured by Motroller Co., for example, and as the dial pulse generator 42 may be used type MC14408 or MC144091C manufactured by the same company. In response to the building up of the key-on signal ST, the latch circuit 45 continuously applies a key detection strobe signal STH to the I-O device 31 until it will not be supplied with a strobe release signal STEN from the I/O device 31 until it will not be supplied STH, the microprocessor 30 executes a predetermined processing to be described later and then stops application of the strobe release signal STEN to the latch circuit 45 and the AND gate circuit 44 to prepare for the next key depression processing. When supplied with the strobe release signal STEN generated during the dial control processing of the microcomputer 30 following the hook-off, the AND gate circuit 44 is maintained in its enabled state until supply of the strobe release signal is stopped at a timing described above. When supplied with a key-on signal ST from the encoder 41, the AND gate circuit 44 applies this signal to the buffer circuit 43 as a strobe signal, while the number signal DN is loaded in the buffer circuit 43. The buffer circuit 43 comprises a number of steps, for example 16. The dial pulse generator 42 forms a series of dial pulses corresponding to the number signal DN stored in the buffer circuit 43 based on the output of an oscillator 41 and sends out the dial pulses in a first-in-first-out mode. At this time, the dial pulse generator 42 produces dial pulses each having a predetermined make time, a break time and a pause time, the number of pulses corresponding to the digit of the depressed key. For example, the make time equals 33 milliseconds, the break time equals 66 milliseconds and the pause time equals to 800 milliseconds.

The dial pulse corresponding to the depressed key is sent to the dial pulse sending out circuit 18 of the dial circuit 26 to open and close a dial contact Di.

The I/O device of the microprocessor 30 is supplied with a coin detection signal CDS from a well known coin detection circuit (CDT) 54 provided for a coin passage, not shown, for applying, if necessary, a coin receiving signal CH to a coin receiving circuit (CHT) 56 for receving coins accumulated in the coin passage, not shown, in a coin box. One end of a hook switch HS2 supplied with the source voltage V through a resistor is connected to the I/O device I/O. Under a normal state, that is hook-on state, the hook switch HS2 is grounded, so that the I/O device produces a high level hook-off signal FHS at the time of hook-off.

The operation of the public telephone set described above will now be described in detail with reference to Figs. 4, 5 and 6.

Under the hook-on state, since the hook switch HS1 is open, the DC loop circuit between the office line terminals L1 and L2 and the speech circuit would not be established. However, the output

voltage V' of the source circuit 20 is applied to the microprocessor 30 to back up the variable memory device 34.

Under this state, when a handset, not shown, is hooked off, the hook switch HS1 is closed to form the DC loop circuit described above so that the telephone exchange is informed of the fact that the handset has been hooked-off. Upon closure of the hook switch HS1, the output of the diode bridge circuit 16 is supplied to the source circuit 20 via the hook switch HS1 and the dial pulse sending out circuit 18 to cause the source circuit 20 to produce voltages V and V' through a well known C.R. charging and smoothing circuit, not shown. These source voltages V and V' are supplied to other component elements of the telephone set to operate them.

When supplied with the source voltage V, the microprocessor 30 judges that the handset has been hooked-off to execute step 1 shown in Fig. 1. More particularly, the CPU 32 accesses the fixed memory device 33 shown in Figs, 1 and 2 to initialize the contents of respective 8 bit registers of the variable memory device 34 and the latch circuit of the I/O device 31, etc., shown in Fig. 1 in accordance with an initial set instruction of a memory region 33a shown in Fig. 2. For example, a signal "FF" is loaded in respective registers 34a through 34m to send a dial permitting signal DEU to the dial pulse generator 42 via the I/O device 31 to enable the buffer circuit 43. Upon completion of the initialization operation, the CPU 32 accesses the memory region 33b of the fixed memory device 33 to execute a self-diagnostic step 102 shown in Fig. 4. At this step 102, a judgment is made as to whether there is a fault or not according to the outputs of sensors located at various portions of the telephone set or the states of various circuits. The results of the judgments are successively stored in a register 34a of the variable memory device 34 shown in Fig. 1. When all self-diagnostic processing results are obtained at step 103, a judgment is made as to whether the speech system is faulty or not depending upon the processing results.

Where there is a fault in the speech system, the CPU 32 accesses again the memory region 33b to execute the self-diagnostic processing. When there is no fault in the speech system, the memory region 33c of the fixed memory device 33 shown in Fig. 2 is accessed to execute the dial control processing at step 105.

When there is no fault in the speech system, the CPU 32 accesses the memory region 33d of the fixed memory device 33 to execute the dial control processing at step 105 shown in Fig. 4 in the same manner as above described. The detail of step 105 is shown in Fig. 5 in which the CPU 32 firstly checks whether there is a dial control termination flag in the register 34b of the variable memory device 34 or not.

When there is the dial control termination flag the program is advanced to the next step 106 shown in Fig. 4. If there is no such flag, the program is advanced to the step 152 shown in Fig. 5 at which the CPU 32 establishes a strobe release signal flag in the register 34c of the variable memory device 34 and sends a strobe release signal STEN to the latch circuit 45 and the AND gate circuit 44 via the I/O device. Thereafter, the program is advanced to step 153 and the CPU 32 judges whether a dialing operation has been made or not. This judgment is made for the purpose of checking whether a strobe signal STH has been sent or not from the dial control circuit 40 via the I/O device 31.

When the result of judgment shows that the strobe signal STH is not sent, and the dialing operation has not been made, the program of CPU 32 advances to step 106 shown in Fig. 4. On the other hand, then the strobe signal STH has been sent, the program is advanced to step 154 shown in Fig. 5. The relationship between the output of the keyboard 50 and the operation of the dial control circuit 40 when the dial is operated will now be described.

When a key of the keyboard 50 is depressed, matrix lines 3 and 4 corresponding to the depressed key send a signal to the encoder 41 of the dial control circuit 40. In response to this signal, the encoder 41 sends a digital signal corresponding to the number of the depressed keys to the buffer circuit 43 and the I/O device 31. Concurrently with the sending out of the digital number signal DN1 the encoder 41 sends a key-on signal 55 to the AND gate circuit 44 and the latch circuit 45. Since the AND gate circuit 44 and the latch circuit 45 are supplied with a strobe release signal STEN at this time, the AND gate circuit as the latch circuit 45 respectively receive a key-on signal ST whereby the latch circuit 45 sends a strobe signal STH to the I/O device 31, while the AND gate circuit 44 sends a strobe signal to the buffer circuit.

Consequently, when a strobe signal STH is detected at step 152, the program is advanced to step 154 described above so as to load a digital signal DN via the I/O device, and to store a dial number DN in the register 34d of the variable memory device 34. When the CPU 32 confirms that the dial signal DN has been stored in the register 24d, the program is advanced to step 155 to reset the flag of the strobe release signal STEN that has been stored in the register 34c of the variable memory device 34. Consequently, the strobe release signal STEN that has been sent to the latch circuit 45 and the AND gate circuit 44 via the I/O device 31 is terminated. As a consequence, the latch circuit 45 stops sending out of the strobe signal STH, and the AND gate circuit 44 stops supply of the strobe signal. Thereafter, even when a dial number signal is sent to the buffer circuit 43, the signal would not be stored therein until the next strobe release signal is supplied to the AND gate circuit 44.

While the AND gate circuit 44 is sending out the strobe signal, a dial number signal DN is loaded in the buffer circuit 43. When supplied with this dial number signal DN, the dial pulse generator 42

converts this signal into parallel series form according to the output of the oscillator 46 to send a dial corresponding to the dial number signal DN to the dial pulse sending out circuit 18 in the first-in-first-out mode to interrupt the dial contact thereby sending out dial pulses to the telephone exchange via the office line terminals L1 and L2.

When the CPU 32 stops the sending out of the strobe release signal STEN, the program is advanced to a parity processing step 156, which constitutes one of the features of this invention, and the detail thereof is shown in Fig. 6. This parity processing step 156 is stored in the memory region 33d of the fixed memory device 33 as a subroutine of the digital control processing. In the parity processing, at first, the group counter 34e of the variable memory device 34 is cleared and its state is changed from "IF" to "00". This group counter has a two bit construction, for example, and a state of this counter 34e of "00" means that rate free number has been selected, whereas a state of this counter of "01" means that an inhibited number has been selected. When the state of the counter is "10" that is it is loaded with [2], it means the count end. The detail of the operation of the counter 34e will be described later.

After clearing the counter 34e, the program is advanced to step 201 where the CPU 32 accesses the memory region 33e of the fixed device 33 to set an address for storing a specific dial number.

In this example, the memory region has an 8 bit construction and in which are stored specific dial numbers of the types shown in the following Table I. The specific dial numbers are classified into a rate free number group and an inhibited number group and each number is stored with data assigned to corresponding addresses.

TABLE I

rate free number			inhibited number		
address	data	number	address	data	number
00	01		0C	01	
01	06	160	0D	00	100
02	F0		0E	F0	
03	01		0F	01	
04	06	165	10	02	122
05	F5		11	F2	
06	01		12	EE	
07	06	166			
08	F6				
09	01				
0A	F5	15			
0B	EE				

For example, the rate free number group is assigned to addresses 00 through 09, 0A and 0B, while the inhibited number group is assigned to addresses 0C through 0F, 10 11 and 12. For example, the rate free number [160] is stored in the addresses 00—02 as date 01, 06 and F0. In this case, the symbol F of "F0" at the third order of magnitude represents an order end code representing that the order of magnitudes terminates. In the same manner, data corresponding to rate free numbers [165], [166] and [15] are stored in addresses 03 through 0A. The last address 0B stores a group end code "EE".

In the same manner, with reference to the inhibited number group, data "01", "00" and "F0" corresponding to an inhibited number [100] are stored in addresses 0C, 0D and 0E, while data [01], [02] and [F2] corresponding to an inhibited number [122] are stored in addresses 0F, 10 and 11. The last digit "F" of the data of respective numbers depresents the order end code, and a group end code "EE" is stored in the address 12.

After the group counter 30e has been cleared, the CPU accesses the memory region 32d for setting the rate free number storing address "00" of the memory region 33e corresponding to the

content "0" of the counter 34e in the working register 335 of the variable memory device 34. Then, at step 202 an address storing the dial number signal DN which has been stored in the register 34d of the variable memory device 34 is set in a register 33g, thus determining a comparison start position of the data for executing the next comparison processing. At this position, the CPU 32 execute the comparison processing of the contents of the registers 33f and 33g at the step 203. When the data in the addresses designated by the registers 33f and 33g do not coincide with each other, a noncoincidence flag is established in a register 33h. On the other hand, when the data coincide with each other no processing is executed.

Then, the program is advanced to step 204 to check whether the data of the compared addresses contain "F" of the order end code or not. If "F" is not contained, the program is advanced to step 205, and the count of an address counter contained in the CPU 32 is incremented to return to step 203 for comparing data stored in address 01 of the next memory region 33c with the data in the next address of a corresponding register 34d. Thereafter, data of respective orders of magnitude are compared with each other.

When an order end code is detected at step 204, the program is advanced to the next step 206 where a judgment is made as to whether a noncoincidence flag is formed in the register 33h of the variable memory device 34 or not. When no coincidence flag is formed, at step 208 a noncoincidence flag is set in a register 33i and then the step is advanced to step 157 shown in Fig. 5. When there is a noncoincidence flag, the program is advanced to step 210 to check whether the group end code "EE" has been detected or not.

Where the group end code is not detected at this step, the program is transferred to step 212 to judge whether the group counter 34e is at its end (10) or not.

At step 210, when the group end code "EE" is detected, the program is transferred to step 211 for incrementing one step the group counter 34e shown in Fig. 3. At this time, since the content of the group counter 34e is "00" the count thereof would be incremented to "01". Then, at step 212, since the content of the group counter 34e has become to the count end of "10", the program is advanced to step "202" at which the content of the register 34d is reset in the working register 33 g of the variable memory device 34 to eexecute the same processing as has been described above with reference to the inhibited number group.

When the group end code "EE" of the address 12 is detected at step 210, the content of the group counter 34e is incremented again to "10". Since this content "10" means the group counter end, the program is transferred to step 157 shown in Fig. 5 via step 212.

At step 157, the CPU 32 accesses the register 34d of the variable memory devices 34 to check whether the first order of the dial order signal stored is "0" or "1" or different therefrom or not. This judgment is made for the purpose of discriminating a specific dial number from other numbers because the first order of the specific number is "0" or "1". When the first order of the specific number is "0" or "1", the program is advanced to step 158. Otherwise, thr rate number processing is executed at step 168. In the same manner as at step 157, at step 158 the CPU 32 accesses the register 34d of the variable memory device 34 to check whether the number of orders of the stored dial number signal DN is larger than 4 or not. When the number of orders is larger than 4, the signal DN is judged that it is not a specific dial number that is a number that requires the user to pay a rate, and the program is jumped to a step 160 to be described later. If the number of orders is less than 4, the program is transferred to step 159.

At step 159, the CPU 32 checks whether there is a coindence flag in the register 33i or not. If there is no flag the program is jumped to step 106. No coincidence flag means that the dial number signal DN is a number other than a rate free number and an inhibited number, that is a rate number as will be discussed later.

When there is a coincidence flag in the register 33i at step 159 the program is advanced to step 160 and succeeding steps to execute processings regarding a rate free number and an inhibited number and the checking of the coins.

At step 160, when the content of the group counter 34e is "00", it means that when a result of comparison of the rate free number with a dial number, the later coincides with either one of rate free numbers [10],[165], [166] and [15] so that the flag register 34i forms a flag. Then, at step 161, a rate free number flag is established in the register 34j of the variable memory device 34. Then, at the next step 162, a dial control end flag is established in the register 34b of the variable memory device 34.

At step 160, when the content of the group counter 34 is not "00" the program is advance to step 164 where a check is made whether the content of the group counter 34 is "01" or not. If the result of the check is YES, it means that the result of comparison of the inhibited number with a dial number shows that the latter coincides with either one of the inhibited dial numbers [100] and [122] so that a flag is established in the coincidence flag register 34i. Then, at step 165, an inhibited number flag is established in the register 34k of the variable memory device 34. Then at step 166, a forced interruption flag is established in the register 34m of the variable memory device 34 and the program is transferred to step 162.

At step 164, when the content of the group counter 34e is not "01", a coincidence flag would not be established in the register 34i, while a coincidence flag is established in the register 34k judging that

this dial number is a rate number so that a rate number flag is established in the register 340. Then at step 169, a judgment is made as to whether there is a signal from the coin detection circuit 54. When there is no coin, at step a dial forced interuption flag is established in the register 34m. At step 169, when there is a coin, the program is transferred to the step 106 shown in Fig. 4.

At step 106, a judgment is made with the CPU 32 as to whether there is an inhibited number flag in the register 34k or not. If the result is YES, at step 108, a loop interruption processing is executed at this time, the CPU 32 sends a loop forced interruption signal FCH to the dial pulse sending out circuit 18 via the I/O device 31 to interrupt the DC loop. Then, at step 109 a post processing is executed. For example, the CPU 32 accesses a coin return circuit, not shown, via the I/O device to return coins accumulated in the coin passage and after confirming that the hook switch HS2 has been closed (hook-on) executes a series of originating processings for preparing the next hook-off.

Where there is no inhibiting flag in the register 34k at step 106, at step 110 a judgment is made as to whether there is a dial control end flag in the register 34k of the variable memory device 34 or not.

When there is no dial control end flag, the program is jumped to step 112, whereas when there is the flag, the program is transferred to step 11 where a judgment is made as to whether there is a rate free number flag in the register 34j of the variable memory 34 or not. When the result is NO, at step 108 a loop interruption processing is executed. On the other hand, when the result is YES, at the next step a judgment is made whether there is a fault or not. This step 112 is executed by checking the result of the self-diagnosis stored in the register 34a of the variable memory device 34. If there is a fault, the program is returned to step 102, instead of advancing to the succeeding steps, for executing again the self-diagnostic processing.

If the telephone set is not faulty, that is normal, the following processing steps are executed. More particularly, after executing the step for the self-diagnosis and step 103 for checking the fault of the telephone set, as has been described hereinabove, the program is advanced to the step 105 for the dial control processing. More particularly, following the steps 151 and 152, if the dial is not operated at step 153, the program is jumped from step 153 to step 106 shown in Fig. 4, and the program is returned to step 112 via step 106 through 111. In this case, since the telephone set is not faulty, the program is transferred to step 114 different from the faulty case.

At step 114, the CPU 32 checks whether the hook switch HS2 is in a hook-off state or not. When the result is YES, the program is transferred to step 115, whereas when the result is NO, at step 108 a loop interruption processing is executed. This step is included at this position of the program because a rate processing is to be executed as will be described later.

At step 115, the same processing at step 105 is executed so that its detail is omitted. After completing the processing at step 162 shown in Fig. 5, at step 116 a check is made whether there is a flag in the register 34k of the variable memory device 34 or not. If the result is YES, at step 108, a loop interruption processing is executed, whereas when the result is NO, at the next step 117, a check is made as to whether there is a flag in the register 34j of the variable memory device 34 or not. When the result of this check is YES, at step 122 a speech state is established without executing the succeeding rate processing.

If the result at step 117 is NO, at step 119 a judgment is made as to whether there is a dial control end flag in the register 34b of the variable memory device 34 or not. When the result is NO, the program is returned again to step 115 to restart the dial control processing. When the result is YES, at step 120 a judgment is made whether a rate signal has received from the rate signal detection circuit 12 or not. When no rate signal was received, the program is returned to step 114, whereas when the rate signal was received, the program is transferred to step 121. Then, the CPU 32 stops to send a dial permission signal DIEN to the dial pulse generator 42 via the I/O device 31 to disenable the buffer circuit 43 and this state is maintained until the next initialization. Then, the program is transferred to step 122 for executing a rate signal processing. In this case, the CPU 32 sends a coin receiving signal CH to the coin receiving circuit CHT via the I/O device to collect the coins in the coin passage into the coin box. Then, at step 123, a speech state is established.

Summarizing the processings described above, when the telephone set is not faulty, that is normal, the following steps are executed. More particularly, after executing the initialization processing step 101 following hook-off, the self-diagnosis processing step 102, speech system fault checking step 103, the dial control processing is executed at step 105. Immediately after the hook-off, since there is no dial control end flag, at step 152, a strobe release signal STEN is sent out and the program is transferred to step 153. Usuall, there is a certain time between the hook-off and a key depression, so that immediately after the hook-off, the result of judgment at step 153 is NO and the program is jumped to step 106 shown in Fig. 4. After executing steps 106 through 114, at step 115 the same processing as at step 105 is executed. Where no dial is operated, the step is advanced to step 119 via steps 116 and 117 at steps 119, a judgment is made again as to whether there is a dial control end flag or not, and when the result is NO, the program is returned to step 115 and the processings are executed again at the following steps. The operations described above are repeated until a dialing operation is made when a dial is operated, at step 115 a predetermined dial control including a parity processing is performed. When the dial number is an inhibited number, the program is transferred to the loop interruption processing step 108 via step 116, whereas when the dial number is a rate free number, the program

jumps to step 122 to establish a speech state. When the number is a normal rate number, a speech state would be established after executing steps 119, 120, 121 and 122.

When a fault is detected as a result of the self-diagnosis processing at step 102, even when a coin clogs the coin passage, unles the speech system is not faulty, it is possible to inform to related offices that the speech is urgent or to inform to the telephone exchange the fact that there is a fault. Accordingly, in the telephone set according to the invention, when the result of self-diagnosis shows that the speech system is not faulty, a signal regarding a rate free speech can be sent by processings executed at steps 105 throgh 111. Of course, during the sending out of such rate free speech signal, it is necessary to inhibit sending of an inhibition signal. To this end, processing steps of 106 through 108 are provided.

Where there is a fault, it is checked at step 112 and the succeeding steps are not executed, and at step 102 the self-diagnosis processing is initiated.

As can be clearly noted from the foregoing description it is possible to determine such specific dial numbers as a rate free number and an inhibited number to any number by changing the content of the memory region 32e of the fixed memory device 33 depending upon the type of processing and the number of orders or digits. To change these numbers, it is necessary to provided additional addresses for the fixed memory device ROM and to determine the full count number of the group counter, but various modifications are possible by determining the control of a rate free speech, a loop interruption, etc., according to the nature of processings.

– When the fixed memory device ROM is constructed to be freely dismountably as by using sockets, it becomes possible to set any specific dial number and the control corresponding thereto by exchanging the ROM so that it is possible to install the public telephone set at any desired position and the setting of a specific dial number and the control content thereof are greatly facilitated.

As above described, according to this invention, a parity check of a sent out dial number and a specific dial number is made correctly and the control based thereon is also made positively. In addition, settings of a specific dial number and the control content thereof can be made readily, so that the public telephone set of this invention can be used widely for many applications.

Although in the charts shown in Figs. 2 and 3 certain numbers of the memory regions have been shown it should be understood that there are many other memory regions.

Fig. 7 is a block diagram showing another embodiment of the telephone set according to this invention in which the same or similar elements are designated by the same reference characters as in Fig. 1. The circuit shown in Fig. 7 is different from that shown in Fig. 1 in that a different type dial control circuit 40A is provided. When supplied with a depressed key signal from the keyboard 50 through 3 x 4 output lines, the dial control circuit 40A outputs a serial dial pulses DP corresponding to a depressed key and a shunt signal Ds. Like that shown in Fig. 1, the dial control circuit 40A is constituted by a pulse generator including a combination of an encoder, a buffer circuit supplied with an output thereof and an oscillator. A type MK 50982 IC sold by Mostec co., is suitable for the dial control circuit 40A.

The dial pulse DP outputted from the dial control circuit 40A is sent to the dial pulse sending out and forced interruption circuit 18 to cause the dial contact Di to interrupt so as to send out dial pulses through the office line terminals L1 and L2. These dial pulses are also stored in the variable memory device 34 via the I/O device 31 of the microprocessor 30. The dial pulses are sequentially compared with such specific dial numbers as the rate free number and the inhibited number stored in the fixed memory device 33. When the dial number coincides with an inhibited number of the specific dial numbers, a loop interruption signal FCH is sent to the dial pulse sending out circuit 18 via the I/O device 31 to forcibly interrupt the DC loop. When the specific dial number is a rate free number the rate processing step is jumped to establish a speech state.

The shunt signal produced by the circuit 40A short circuits the input terminals of the speech circuit 24 so as to prevent pulse noise produced at the time of sending out the pulses from affecting the speech circuit just in the same manner a sin the embodiment shown in Fig. 1. The dial permission or enabling signal DIEN sent from the I/O device 31 to the dial control circuit 40A is generated when a rate signal is received from the telephone exchange, not shown, via a rate signal detection circuit or when the dial pulses DP do not coincide with the rate free number to prevent generation of the next dial pulses.

Fig. 8 shows still another embodiment of this invention in which identical or similar elements to those shown in Fig. 1 are designated by the same reference charactors. The embodiment shown in Fig. 8 is different from that shown in Fig. 1 in that 3 x 4 output lines of the keyboard 50 are connected to a dial control circuit 40B and also to the I/O device 31 of the microprocessor 30.

The dial control circuit 40B is constructed to produce a multifrequency signal MF corresponding to a depressed key signal sent from the keyboard 50 over 3 x 4 output lines and a shunt signal DS. The multifrequency signal MF corresponds to respective keys and have different frequencies. As the dial control circuit 40B may be used type 5089 IC sold Mostec Co. The multifrequency signal MF generated corresponding to the depressed keys is sent to the shunt circuit 22A.

The shunt circuit 22A comprises a transfer switch SW that transfers the circuit between a circuit forming the DC loop to the speech circuit 24 and a circuit that short circuits the input terminals of the

speech circuit 24, an amplifier AP connected in series with the shunt circuit and a transformer TR connected on the input of the amplifier. The multifrequency signal MF outputted from the dial control circuit 40 is supplied to the office lines via the transformer TR, amplifier AP and transfer switch SW of the shunt circuit 22A to act as a multifrequency dial signal.

The transfer switch SW is transferred by the shunt signal DS outputte dby the dial control circuit 40B to disconnect the speech circuit at the time of transmitting the multifrequency signal MF.

The depressed key signal from the keyboard 50 is stored in the variable memory device 34 via the I/O device 31. Like the embodiment shown in Fig. 1, if necessary, the depressed key signal may be converted into a digital dial number and then sent to the variable memory device 34. The depressed key signal or a digital dial number stored in the variable memory device 34 is compared with such specific dial numbers as a rate free number and the inhibited stored in the fixed memory device 33. When these compared signals coincide with each other, and in the case of a rate free telephone set, the CPU 32 jumps over the rate processing step, or in the case of the inhibited number, the CPU 32 sends a forced interruption signal FCH to the forced interruption circuit 18A to forcibly interrupt the DC loop. In this embodiment, the circuit 18A is different from those of the foregoing embodiments in that it does not contain a dial pulse sending out circuit.

Fig. 9 shows still another embodiment of the public telephone set according to this invention which is constructed to load a dial number signal in a microcompressor and after completing a parity processing, a dial signal is sent out to the office lines according to the result of the parity processing. Elements shown in Fig. 9 identical to those shown in the foregoing embodiments are designated bv the same reference charactors. In this modification, a depressed key signal outputted from the keyboard 50 is sent to an encoder 41 of a dial control cictuit 40C to be converted into a 4 bit dial number signal DN which is then stored in the variable memory device 34 via the I/O devices 31. The encoder 41 also produces a key-on signal at the time of building up of the depressed key signal and sends a strobe signal STH to the I/O device through the latch circuit 45. The succeeding processings executed by the microprocessor are the same as those of the embodiment shown in Fig. 1 up to the parity processing.

In this embodiment, the dial control circuit 40C comprises a first pulse generator 42A and a second pulse generator 42B.

The first pulse generator 42 has the same construction as that shown in Fig. 8 and when enabled by a selection signal MFENA, the first pulse generator 42 sends a multifrequency signal MF and a shunt signal DS1 to the shunt circuit 22B based on an input signal KYOUA. Like the previous embodiment, the pulse generator 42 may be formed of type 5089 FC sold by the MOSTEC Co. In the same manner as in the foregoing embodiment, when the result of comparison of the content of the variable memory device 34 storing the output of the encoder 41 with the content of the fixed memory device 33 shows that the number is a specific dial number other than an inhibited number or an ordinary rate number dial, input signal KYOUA is converted into signal corresponding to those signal that is an output signal from the keyboard 50 and then sent out through the I/O device 31.

The second pulse generator 42B has the same construction as that shown in Fig. 7 and sends serial dial pulse signals DP and a shunt signal DS2 to a shunt circuit 22B based on the input signal KYOUB. The generator 42B may slso be constituted by the type MK50992IC sold by the MOTROLA Co. When the result of comparison of the content of the variable memory device 34 storing the output of the encoder 41 with the content of the variable memory device 34 shows that the number is a specific number other than an inhibited number or an ordinary rate dial number, the input signal KYOUB is converted into a signal corresponding thereto, that is a signal corresponding to the 3 x 4 output signals outputed from the keyboard 50 and the converted signal is sent out from the I/O device 31.

Similar to that shown in Fig. 8, the shunt circuit 22B comprises a transfer switch SW1 that transfers the connection between a circuit that forms the DC loop to the speech circuit 24 and a circuit that shunts the input terminals of the speech circuit 24, an amplifier AP included in the shunt circuit, and transformer TR provided for the primary side of the transformer Tr. The multifrequency signal MF sent from the first pulse generator 42A is applied to the office line to act as the dial signal through the transformer TR, amplifier AP and diode bridge circuit DD and the transfer switch SW of the shunt circuit 22B.

The transfer switch SW1 is actuated by the shunt signal DS1 sent from the first pulse generator 42A to disconnect the speech circuit 24 at the time of sending out the multifrequency signal MF in the same manner as in the foregoing embodiment.

The shunt circuit 22B further includes a second transfer switch SW2 that transfers the connection between a circuit forming a DC loop and a circuit that shunts the input terminal of the speech circuit whereby when the second pulse generator 42B outputs dial pulses the pulse noise is prevented from affecting the speech circuit 24. An integrated circuit comprising a combination of the shunt circuit 26 having the construction described above, and a speech circuit 24 is sold by ITT Co. under a trade name of the type TEA — 1045 IC.

When the movable contact of a transfer switch SWT is thrown to a stationary contact (DP) PS, the microprocessor 30 detects this state via the I/O device and the CPU 32 judges that the second pulse generator 42B has been selected.

Then, a selection signal DPENA is sent to the second pulse generator 42B via the I/O device 31 to

enable the second pulse generator 42B. Then, when a key of a keyboard 50 is depressed, a dial number signal DN corresponding to the depressed key is sent to the variable memory device 34 via the encoder 41. The dial number is compared with a specific dial number stored in the fixed memory device and the result of comparison is stored in a predetermined register of the variable memory device. The following Table II shows the contents of the specific dial numbers stored in the fixed memory device wherein (1) represents two inhibited numbers, (2) two rate free numbers, (3) a single tall office number, (4) three conversion numbers and (5) a plurality of local numbers.

TABLE II

Processing	Address	Data	Number	Processing	Address	Data	Number
inhibited number	00	00		conversion number	14	00	
	01	00	1020		15	00	000
	02	02			16	F0	
	03	F0			17	00	
	04	01			18	00	003
	05	09	190		19	F3	
	06	F0			1A	01	
	07	EE			1B	00	109
rate free number	08	01			1C	F9	
	09	00	1022		1D	EE	
	0A	02		local office number	1E	F2	2xx
	0B	F2			1F	F3	3xx
	0C	00			20	F4	4xx
	0D	09	093		.	.	
	0E	F3			.	.	
	0F	EE			.	.	
toll office number	10	00			.	.	
	11	09	090		.	.	
	12	F0			25	F9	9xx
	13	EE			26	EE	

In this table the letter F represents the end code at the last order of each number, while EE represents the group end code of the last order of each group number.

The comparison processing of this modification is identical to that of Fig. 1 but as the number of types of the specific dial numbers is increased, it should be understood that the count of the group counter 34e shown in Fig. 1 should be increased correspondly.

When the dial number of a depressed key is an inhibited number, the CPU 32 sends a loop interruption signal FCH to the dial pulse sending out and the forced interruption circuit 18 via the I/O device 31 to interrupt the DC loop. On the other hand, where the dial number of a depressed key is a rate free number the dial number signal is applied to a conversion table contained in the fixed memory device 33 to convert it into the input signal KYOUB applied to the second pulse generator 42B.

When the depressed key dial number is a toll office number, the code of the dial number is converted into the input signal KYOUB similar to the rate free number described above.

When the depressed key dial number is a converted signal the CPU 32 accesses a data conversion table stored in the fixed memory device, and after converting the dial number into specific numbers such as 001, 101, etc., the code of the specific number is converted to form an input signal KYOUB in the same manner as the rate free number and the toll office number described above.

Where the depressed key dial number is a local number, after confirming the presence or absence of a coin, the code of the dial number is converted to form the input signal KYOUB to the second pulse generator 42B.

The comparison is made only for the first order and the second and following orders are neglected.

When the second pulse generator 42B receives this input signal it produces a serial dial pulses DP and a shunt signal DS2 related thereto based upon the input signal KYOUB which are sent to circuit 18 and the shunt circuit.

When the movable contact of the transfer switch SWT is thrown to the stationary contact (MF)FS, the microprocessor 30 detects that the first pulse generator 42A has been selected and sends a selection signal MFENA to the first pulse generator 42A via the I/O device 31 to enable the first pulse generator.

Subsequent dial control operations including a parity processing is the same as a case where the second pulse generator 42B is selected.

According to the input signal KYUOUA sent through the I/O device 31, the first pulse generator 42A forms a multifrequency signal MF and a shunt signal DS1 which are applied to the shunt circuit 22B.

It should be understood that the invention is not limited to the specific embodiment described above, and that a number of changes and modifications will be obvious to one skilled in the art.

Although in the foregoing embodiments, a judgment is made whether the dial number storeed in the various memory devices coincides with a specific dial number lastly stored in the fixed memory device at a time when all digit signals of the dial number have been stored in the variable memory device, it is also possible to sequentially compare the dial number signal stored in the variable memory device with respective digits of a specific dial signal stored in the fixed memory device, thus sequentially executing parity processings of respective orders or digits starting from the first order.

CLAIMS

1. A public telephone set comprising:

a keyboard including a plurality of keys;

a first memory device for storing a signal related to a dial number produced as a result of operation of a said key;

a second memory device for storing a predetermined specific dial number;

a control unit for comparing contents of said first and second memory devices according to a predetermined sequence; and

office line originating means controlled by said control unit for controlling transmission of a dial signal corresponding to said specific dial number when the contents of said first and second memory devices coincide with each other.

2. The public telephone set according to claim 1 wherein said specific dial number includes a rate free number and an inhibited number, and wherein said office line originating means comprises means for transmitting a dial signal corresponding to the content of said first memory device to office lines without executing a rate processing when coincided content of said first memory device represents a rate free number, and means for interrupting a DC loop adapted to transmit the dial number when the coincided content of said first memory device represents an inhibition signal.

3. The public telephone set according to claim 1 wherein said office line originating means comprises means for transmitting a dial signal according to a result of comparison of the contents of said first and second memory devices.

4. The public telephone set according to claim 1 wherein said office line originating means comprises means for sending out to office lines a series of dial pulses corresponding to said dial number.

5. The public telephone set according to claim 1 wherein said office line or lighting means comprises means for sending a multifrequency signal corresponding to said dial number to office lines.

6. The public telephone set according to claim 1 wherein said office line originating means comprises first means for sending a series of dial pulses corresponding to said dial number to office lines, a second means for sending a series of dial pulses corresponding to said dial number to office lines, a second means for sending a multifrequency signal corresponding to said dial number to said office lines, means for selecting either one of said first and second means, and means responsive to an output of said selecting means for sending said dial number to said office line via either one of said first and second means.

7. The public telephone set according to claim 5 wherein said memory device stores a depressed key signal as it is, while said second memory device stores a signal corresponding to a specific dial number corresponding to the depressed key signal.

8. The public telephone set according to claim 1 which further comprises an encoder which forms a digital number signal corresponding to a depressed key and wherein said first memory device stores an output of said encoder under the control of said control unit.

9. The public telephone set according to claim 8 wherein said office line originating means comprises means supplied with the output of said encoder for sending out a series of dial pulses to said offices lines and means for controlling sending out of said dial pulses to said office lines in accordance with a predetermined dial number.

10. The public telephone set according to claim 9 wherein said first memory device stores said dial pulses.

11. The public telephone set according to claim 5 wherein said first memory means stores an output of a depressed key and said office line originating means comprises means for sending a multifrequency signal to said office lines based on an output of a depressed key, and means for controlling sending out of said dial pulses to said office lines in accordance with a predetermined dial number.

12. The public telephone set according to claim 1 which further comprises a third memory device which checks a faulty portion according to a predetermined instruction sequence and stores a result of check under the control of said control unit, and wherein said control unit comprises means for comparing the contents of said first and second memory means and transmitting a result of comparison when a result of checking shows that there is no fault in a speech system.

13. The public telephone set according to claim 12 wherein a specific dial number processed at a time when it is determined that there is no fault in the speech system includes at least one rate free number.

14. The public telephone set according to claim 1 or 3 wherein said specific telephone number

further comprises a conversion number and wherein said office line originating means comprises means which when the content of said first memory device coincided with the content of said second memory device comprises the conversion number, converts the same into another number and sends a dial signal corresponding to said another number.

15. A public telephone set substantially as described herein with reference to the accompanying drawings.

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